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MANAGING THE INTERFACE FOR RECEIVING CALLER IDENTIFICATION DELIVERY MESSAGES USING A MICROCONTROLLER (II)

BY

PETRUȚ DUMA[1,*] and EUGEN PETAC[2]

[1]Technical University "Gheorghe Asachi" of Iași,
Faculty of Electronics, Telecommunications and Information Technology,
[2]"Ovidius" University of Constanta,
Faculty of Mathematics and Computer Science

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Abstract. The work presents the physical level specifications for the caller subscriber identification service, the parameters of the signals circulating on the subscriber line, the data transmission and reception using a modem, communication principles and protocols, the messages' structures etc. It is described the hardware structure of the interface for receiving caller identification delivery messages, as well as the main characteristics of the command program required by the application. The program implements various features for displaying messages and for saving them in a non-volatile memory.

Key words: interface for caller subscriber identification; continuous phase binary frequency shift keying modulation; caller identification delivery messages.

1. Introduction

The telephone networks use the Caller Number Delivery (CND) service for transmitting the information regarding the number of the calling subscriber during the first pause of the call signal, or the Caller Name Delivery (CNAM)

[*]Corresponding author: *e-mail*: pduma@etti.tuiasi.ro

service that sends the number along with the name of the calling subscriber. Presently, specialized integrated circuits are available for receiving the caller subscriber identification information using Frequency Shift Keying (FSK) modulation based on standards like Bell 202, ITU-TV-23 etc.

In order to receive the caller subscriber identification information, it is required that the called subscriber connects on the telephone line a specific interface with the basic structure shown in Fig. 1; the acronyms used have the following meaning: TLI – telephone line interface, IRCIDM – interface for receiving caller identification delivery messages; µC_CU – microcontroller based command unit; µC_AS – microcontroller based application system; µC_DS – microcontroller based development system; SI – serial interface; PC – personal computer; RTC – real time clock; FSM – flash serial memory; LCD_DDC – LCD data display console; TS – telephone set; TL – telephone line; TSC – telephone set connector; TLC – telephone line connector.

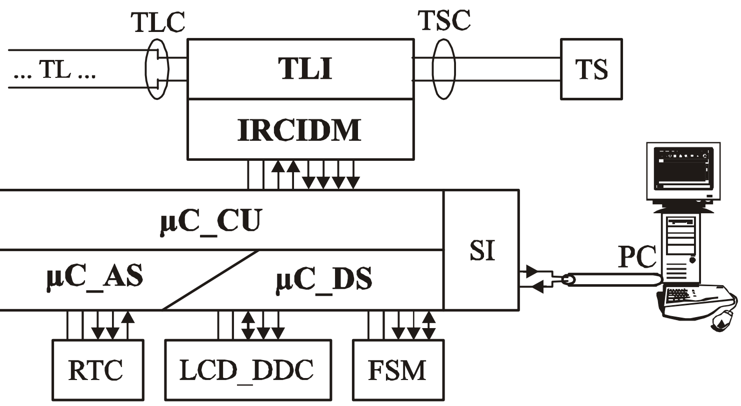

Fig. 1.

The telephone line interface monitors the subscriber line, receives and transmits the selection information, detects the calling signal, receives tones and performs other functions that are not used in this application. The interface for receiving caller ID messages contains basically a FSK decoder that transmits serially the relevant information. The command unit is a development system with microcontroller during the development and testing phases and in the final stage it will become an application system with microcontroller (ATMEL, PIC or any other family).

All the messages provided by the FSK decoder along with other data are loaded in the flash memory. The data display console is a LCD indicating the relevant information for every call.

A previously published paper (Duma, 2015) presented the main functional features of the caller ID module according to Bellcore references. This work presents the hardware structure for receiving FSK messages that identify the caller and the main features of the command program.

2. The interface for caller subscriber identification

The interface is based on the integrated circuit SM8223A produced by Nippon Precision Circuits and basically consists of a FSK decoder and a DTMF (Dual Tone Multi-Frequency) receiver in order to identify the calling subscriber when a call is placed for the called subscriber. The circuit receives at a physical level the signals that are sent by the exchange according to Bellcore specifications.

The main characteristics of this circuit are: – supports caller subscriber identification for FSK and DTMF signals; – includes a FSK decoder and a DTMF receiver, controlled by a FSK/DTMF logical discriminator; – includes a ring detector; – the input has a differential amplifier; – has a serial asynchronous data transmission interface; – features a low consumption operation mode; – uses a single low value DC power supply; – the internal clock oscillator requires a quartz crystal; – is based on CMOS technology.

The device is used in telephony (PABX), fax machines, modems, telephone sets and in any other interface supporting caller ID services.

The internal block diagram of the SM8223A is presented in Fig. 2. The notes have the following meaning: DA - differential amplifier; LD_FSK/DTMF – logical discriminator for FSK or DTMF signals; FSK_Dec – FSK decoder; M_1/M_2 – multipliers; BPF – band pass filter; FSK_LD – FSK logical decoder; SR – serial register; *B* – tri-state buffers; DTMF_Rx – DTMF receiver; DTF – dial tone filter; HGF – high group filter (band pass filter for the DTMF high frequencies group); LGF – low group filter (band pass filter for the DTMF low frequencies group); ST, ST_1, ST_2 – Schmitt triggers; DTMF_LD – DTMF logical decoder; RD – ring detector; *N* – transistor; Osc – Oscillator; PS – power supply, polarizing, power-down (PD) and reference voltage (V_{ref}) circuits.

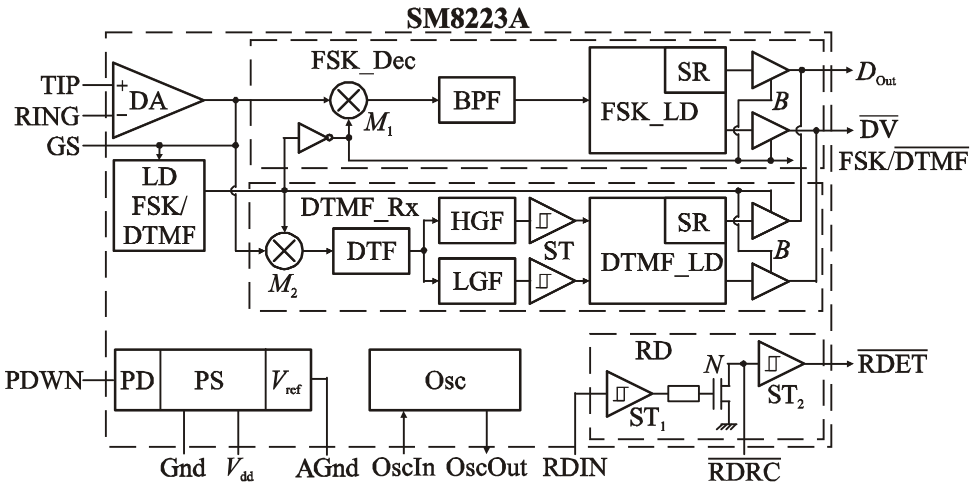

Fig. 2.

The input differential amplifier has the role of setting the useful signal amplification from the telephone line. A single inverter input configuration is possible, but it is seldom used. Generally, an amplifier with differential inputs and a single output is used, in order to perform a symmetrical adaptation with the telephone line (Fig. 3).

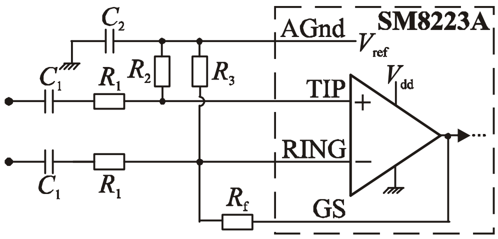

Fig. 3.

The C_1 capacitors allow the useful signal to pass (are “short-circuited”), but in DC they do not allow the subscriber loop from the telephone line to close. A reference voltage decoupling capacitor C_2, connected between AGnd and Gnd is used for bringing the input signal on the reference voltage V_{ref} level. The voltage amplification is calculated by removing from the output the effect of the input polarizing currents.

$$A_V = \frac{R_f}{R_1}, \text{ with } R_2 = \frac{R_f \cdot R_3}{R_f + R_3} \qquad (1)$$

The structure of the amplification circuit used in practice differs from the one presented in the figure above, because this amplifier is reached also by the call signal, that is a high amplitude (tens of volts) sinusoidal signal. In order to protect the input amplifier, a calling signal limitation is necessary (Fig. 4).

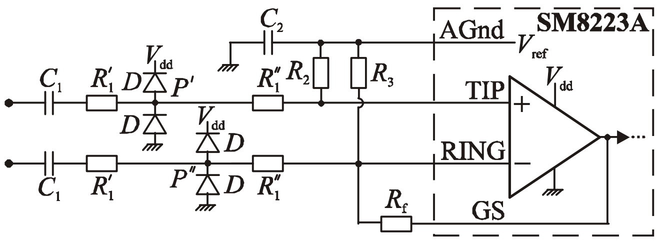

Fig. 4.

Each of the R_1 resistors is divided into two resistors (R_1’ and R_1”) between which two call limiting diodes D are connected:

$$R_1 = R'_1 + R''_1 \qquad (2)$$

When the call voltage in points P’ and P” respectively is higher than Vdd+0.6V or lower than –0.6V, then the corresponding diode D is open and limits this signal, while the amplifier is also limited.

The output of the amplifier is connected to a FSK/DTMF logical discriminator and to two multipliers that lead to the FSK decoder and the DTMG receiver respectively. This discriminator circuit determines whether the input signal is a FSK signal or a DTMF signal by detecting the channel seizure information in the FSK signal header; the circuit also performs an automatic discrimination between the various types of input signals in order to determine if the received FSK signal is within the specifications of Bellcore GR-30-CORE standard.

If the $\mathrm{FSK}/\overline{\mathrm{DTMF}}$ signal provided by the discriminator is a logical 1, then the signal on the telephone line is a FSK signal and it reaches the FSK decoder.

The Bellcore standard for identifying the caller subscriber sets the following characteristics for the physical interface: – continuous phase binary frequency shift keying modulation; – data bit logical 1 (mark) has the frequency of 1,200 Hz ±1%, with the level from –32dBm up to –12 dBm; - data bit logical 0 (space) has the frequency of 2,200 Hz ±1%, with the level from –36dBm up to –12 dBm; – the data transmission is made serially asynchronously with a baud rate of 1,200 bit/s ±1%; - the telephone line has two wires.

The FSK caller ID signal is transmitted from the telephone exchange during the pause between the first and the second call burst and has an amplitude of maximum 200 mV. The transmitted signals sequence is depicted in Fig. 5; the acronyms used have the following meaning: FRB – first ring burst; SRB – second ring burst; NRB – next ring burst; CSS – channel seizure signal; MS – mark signal; DP – data packet; P – pause between two consecutive ring bursts.

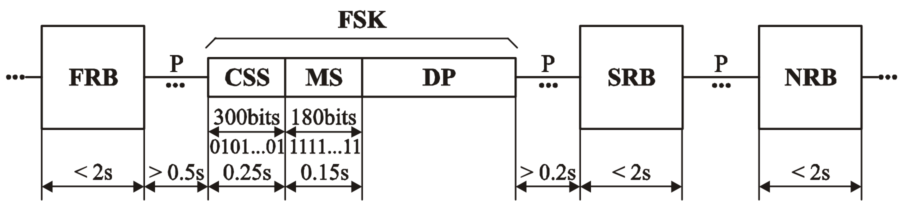

Fig.5.

The ring detector delivers signal $\overline{\mathrm{RDET}}$, active on logical 0 during the transmission of the call signal on the telephone line and on logical 1 respectively while the call signal is not transmitted (Fig. 6).

The first call burst is followed by a pause of at least 0.5 s, then the FSK signal containing the caller ID is transmitted. It starts with the channel seizure signal consisting of the alternative transmission of 300 bits (010101…01) for 0.25 s. Then the mark signal is sent, consisting of transmitting 180 bits with logical value 1 for 0.15 s. In the end, the data package is sent, followed by a pause of at least 0.2 s until the second ring burst starts.

The data validation signal $\overline{\mathrm{DV}}$ is initially in logical 1 and is activated after the reception of the channel seizure signal and at maximum 3.75 ms after the mark signal starts. $\overline{\mathrm{DV}}$ is in logical 0 during the reception of the entire data package and inactive otherwise.

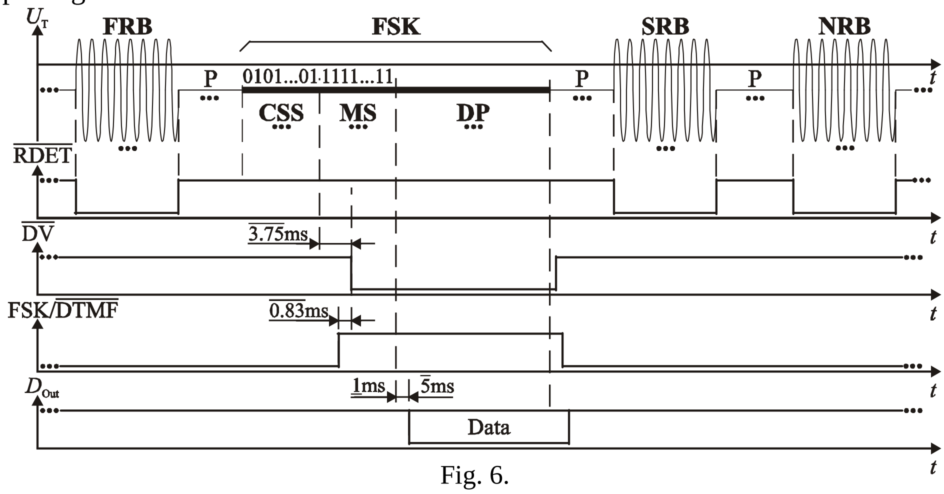

Fig. 6.

The logical discriminator sets the FSK/$\overline{\mathrm{DTMF}}$ signal with maximum 0.83 ms before the activation of the data validation signal; this signal is reset after the data package reception and after the inactivation of the $\overline{\mathrm{DV}}$ signal.

The bytes in the data package containing the relevant information are transmitted serially to output D_{Out}, in the same order as the message, indicating: the type and the length of the message, the type and the length of the parameter, the ASCII codes of the characters holding the date information (day and month), time (hour and minute), number and/or name of the caller subscriber. Any data byte consists of a START bit (logical 0), eight data bits from the less significant bit (LSB) to the most significant bit (MSB) and the STOP bit (logical 1), as in Fig. 7. The serial data provided at output D_{Out} are delayed with a time interval from 1 ms up to 5 ms. There are no pauses introduced between the data in the package and, if the central office has no more data to send or it waits for the information to be validated, then up to 10 bits with logical value 1 may be inserted.

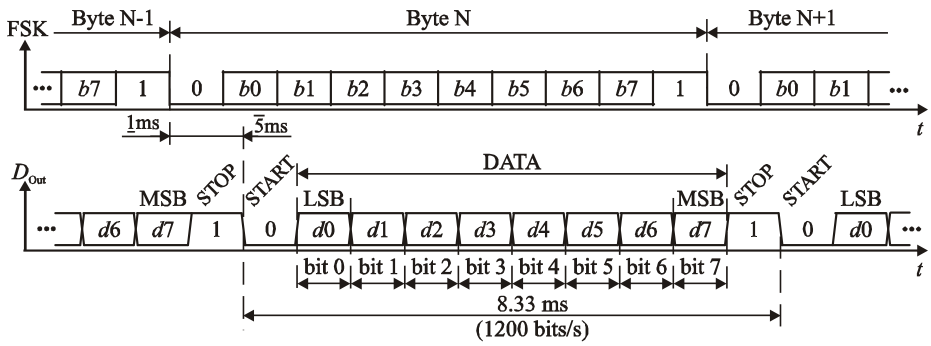

Fig. 7.

If the $\mathrm{FSK}/\overline{\mathrm{DTMF}}$ signal provided by the discriminator is logical 0, then on the telephone line is to be found a DTMF signal that is directed to the DTMF receiver.

The DTMF receiver has a notch filter at its input in order to reject the dialing tone, followed by two band pass filters with switched capacitors. The signals from the low frequency group and of the high frequency group, respectively, are available at their outputs. The two signals are limited using comparators, then they are passed through hysteresis Schmitt triggers in order to prevent the detection of low level signals and of the noise. Using a decoder based on a digital technique, the binary value of the tone is determined and, with an averaging algorithm, a protection against tone simulation is performed. Before storing and serially sending the binary code corresponding to a decoded pair of tones, the validation duration of the received DTMF signal is checked, along with the extent of the following pause.

The call signal arriving on the telephone line in order to notify the called subscriber passes through a protection circuit and is applied to a divider consisting of capacitors C_3, resistors R_5, R_6, R_7 and the rectifier bridge based on diodes *D*' (Fig.8).

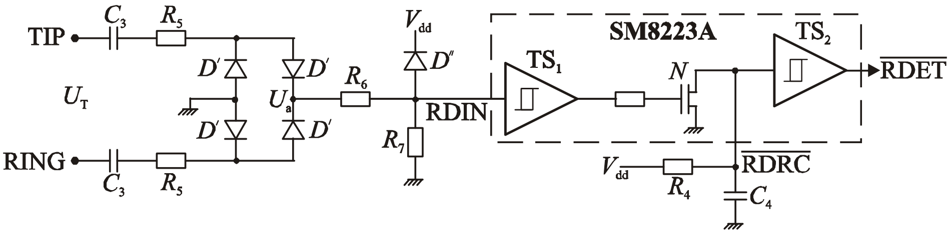

Fig. 8.

The calling signal consists of an AC component having the effective voltage of 80V and the frequency between 20÷50 Hz as it leaves the telephone exchange, added over a DC voltage of –48V and sent in a specific cadence (1.7 s call and 3.3 s pause). At the telephone set's connection terminals, the calling signal (U_T) has a lower amplitude, down to 40÷70 V, due to the voltage drop on the telephone exchange circuits and on the telephone line (Fig. 9).

The DC component is cut by capacitors C_3. The call signal is divided, in the first stage, by capacitors C_3 and resistors R_5 and then it is rectified by the D' diode bridge. The ring detector is controlled by RDIN that is obtained from the preceding signal (U_a) divided by resistors R_6 and R_7. Signal RDIN is obtained by dividing (C_3, R_5, R_6 and R_7) and rectifying U_T signal (the opening voltages of diodes *D*' are negligible).

$$\mathrm{RDIN} = \frac{R_7}{\sqrt{\left(R_5 + R_6 + R_7\right)^2 + \left(\dfrac{1}{\omega \cdot C_3}\right)^2}} \cdot U_\mathrm{T} \tag{3}$$

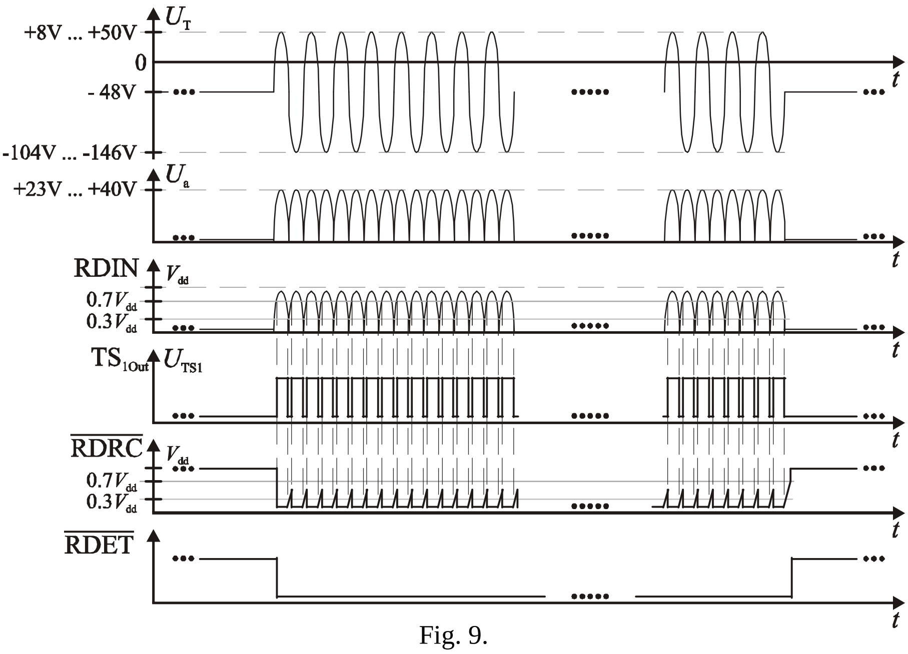

Fig. 9.

For a 50 Hz frequency of the call signal, capacitors C_3 have a negligible impedance compared to the sum of the resistors in the divider (the error margin is under 2%), thus the signal RDIN is calculated using the following relation:

$$\mathrm{RDIN} = \frac{R_7}{R_5 + R_6 + R_7} \cdot U_\mathrm{T} \tag{4}$$

Subsequently, RDIN commands the Schmitt trigger ST_1; as RDIN exceeds the upper threshold ($0.7V_{dd}$), the output passes into logical 1 and when it decreases below the lower threshold ($0.3V_{dd}$), the output passes into logical 0. For a calling signal U_T with the effective voltage higher than 40V, RDIN is higher than 2.1V, and the ring detector works. If the call signal has an effective voltage higher than 68V, then diode *D*” opens and limits this signal.

The output of trigger ST_1 controls transistor *N* as follows: with a logical 1 level, transistor *N* is saturated and short-circuits capacitor C_4, while a logical 0 blocks *N*, which allows capacitor C_4 to load through resistor R_4. The time constant R_4C_4 is calculated from the following equation:

$$R_4 C_4 = \frac{t}{\ln \dfrac{V_{dd}}{V_{dd} - V_{TS}}} \tag{5}$$

where: t is the holding time, while the threshold values of the Schmitt trigger V_{TS} are between $0.3V_{dd}$ and $0.7V_{dd}$.

The linear-variable voltage $\overline{\mathrm{RDRC}}$ commands the second Schmitt trigger (ST_2). If a call is received, these linear-variable voltages have a lower amplitude than the upper threshold ($0.7V_{dd}$) of the ST_2 trigger, therefore the output of the $\overline{\mathrm{RDET}}$ ring detector being in logical 0. If no call is detected, the linear-variable voltage exceeds the upper threshold and switches $\overline{\mathrm{RDET}}$ to logical 1.

The interface structure is based on SM8223A circuit and is connected to the telephone line in order to receive the identification signal of the caller subscriber. This interface is managed by an application system equipped with an ATMEL microcontroller and is shown in Fig. 10.

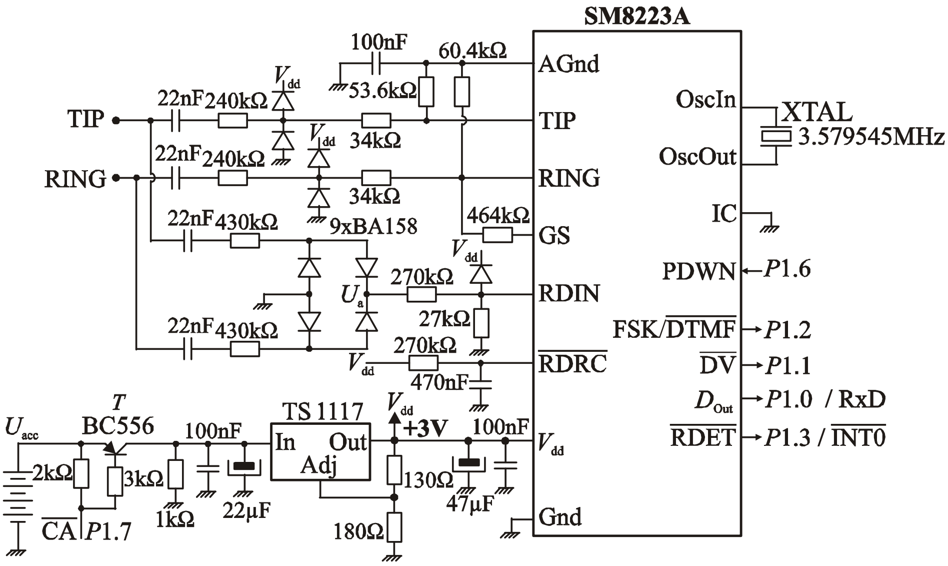

Fig. 10.

The input differential amplifier that provides the relevant signal to either the FSK decoder or the DTMF receiver is interfaced with a circuitry including capacitors, resistors and diodes, as described previously (Fig. 4). Similarly, the ring detector that receives the call signal is interfaced through a structure of capacitors, resistors and diodes, as previously described in Fig. 8.

The internal clock oscillator used for decoding the FSK or DTMF signals requires an external 3.579545 MHz quartz crystal. In order that normal operating processes to be performed, the test input IC is connected to logical 0 (Gnd).

The SM8223A device is powered from a DC voltage of 3V (±10%) that is obtained from four serially connected accumulators. In order to obtain a proper power supply, a three-point adjustable voltage stabilizer (TS1117-Adj) is used, requiring external decoupling capacitors and a resistive divider that sets the power supply voltage to +3V. The control of the power applied to the interface is made using transistor T (BC556); the command signal $\overline{\mathrm{CA}}$ is active on logical 0 and is provided by software on line $P1.7$ of the microcontroller.

This circuit can be set to a power-down operating mode in order to minimize the power drained from the accumulators. Signal PDWN is set to logical 0 for the normal operating mode and to logical 1 for entering the power saving mode. This is achieved by controlling PDWN with line $P1.6$ of the microcontroller, which allows to set the necessary operation mode through software.

The other output signals $\overline{\mathrm{RDET}}$, $\mathrm{FSK}/\overline{\mathrm{DTMF}}$, $\overline{\mathrm{DV}}$ and D_{Out} are managed by lines $P1.3 \div P1.0$ of the microcontroller in order to receive the information.

The command program features several functions. Thus, the call detecting signal $\overline{\mathrm{RDET}}$ can be sampled and analyzed through software or can place an interrupt request ($\overline{\mathrm{INT0}}$) that sets in motion the process of receiving the caller ID information. The $\mathrm{FSK}/\overline{\mathrm{DTMF}}$ signal defines different data interpretation models that must be processed accordingly. The data validation signal $\overline{\mathrm{DV}}$ specifies the fact that the serial data from output D_{Out} must be received either with the serial interface of the microcontroller (RxD) or through software. The use of the serial interface requires a simple program sequence, but there are applications when this interface is not available.

In order to receive data through software, D_{Out} must be sampled and the falling edge of this signal must be detected in order to trigger the start for this process. Then, each bit with the duration of 0.833 ms is sampled with a period 32 times smaller than the bit period. The software sample rate is 26 µs. Between samples 14 through 18, the inputs are loaded and the value of the received bit is decided by a majority logic. For the first bit (START) a logical 0 must be received. If the first received bit is logical 1, which is a false start, then the process is cancelled and the next falling edge is awaited in order to restart it. If the first received bit is logical 0, the data reception process continues. The next received bit is sampled in the same manner, during samples 14 through 18 the inputs are loaded and the value of the bit is decided using the same majority logic and so on. The process is repeated for all the data bits and finally for the STOP bit. The eight received data bits are used to compose the currently received data byte. If the last received bit is logical 1, the data is valid, otherwise an error is considered to have occurred and the data is discarded. In both cases, the process continues with the reception of the following data set.

4. Conclusions

The main physical characteristics of a caller ID system are described. The hardware structure presented was built in practice and, along with an LCD and a flash memory, it is managed by an ATMEL microcontroller. This structure receives all the FSK signals containing relevant information from the telephone line and they process it accordingly.

The command program is written in machine code and receives caller ID information, stores all the relevant information into the flash memory, while for each call, on the LCD, are displayed the date, time, the number of the caller subscriber, his name and other similar information. When there are no messages to display, the console shows the date and time from the local real-time clock. This command program is stored in a 4.7 KBytes program memory area and stands out by the small storage area required compared to the functionalities it features.

The structure can be developed by adding a high capacity flash memory card (GBytes) and by designing the command program to search a database in order to retrieve and display various further information on the caller subscriber. Thus, for instance, an insurance company might use relevant information on the calling client before answering the phone, a family medical practice might use the service to display the health status of the calling patient or a delivery company might already check the status of the current order of the caller subscriber.

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GESTIONAREA INTERFEȚEI PENTRU RECEPȚIONAREA MESAJELOR DE IDENTIFICARE ABONAT CHEMĂTOR CU MICROCONTROLER (II)

(Rezumat)

Lucrarea prezintă specificațiile la nivel fizic pentru serviciul de identificare abonat chemător, parametrii semnalelor vehiculate prin linia de abonat, transmiterea şi recepționarea datelor pe bază de modem, principii şi protocoale de comunicare, structura mesajelor etc. Este descrisă structura hardware a interfeței pentru recepționarea mesajelor de identificare abonat chemător, ca şi principalele caracteristici ale programului de comandă necesar aplicației. Programul implementează diverse facilități pentru afişarea mesajelor şi respectiv pentru salvarea acestora într-o memorie nevolatilă.